Low-k Interconnect Stack with a Novel Self-Aligned Via Patterning Process for 32nm High Volume Manufacturing

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Abstract

Interconnect process features are described for a 32nm high performance logic technology. Lower-k, yet highly manufacturable, Carbon-Doped Oxide (CDO) dielectric layers are introduced on this technology at three layers to address the demand for ever lower metal line capacitance. The pitches have been aggressively scaled to meet the expectation for density, and the metal resistance and electromigration performance have been carefully balanced to meet the high reliability requirements while maintaining the lowest possible resistance. A new patterning scheme has been used to limit any patterning damage to the lower-k ILD and address the increasingly difficult problem of via-to-metal shorting at these very tight pitches. The interconnect stack has a thick Metal-9 layer to provide a low resistance path for the power and I/O routing that has been carefully scaled to maintain a low resistance. The combined interconnect stack provides high density, performance, and reliability, and supports a Pb-free 32nm process.

Introduction

As process dimensions continue to shrink, additional improvements are required to enable high performance logic devices. A full overview of the 32nm process has been given [1]. In this work the performance of the interconnect stack is more fully described.

The dual damascene processing scheme has been extended from previous generations at Metal-1 to Metal-8 with several improvements for increased reliability and performance. At the tightest pitch layers a lower-k CDO and a new hardmask process are utilized. This hardmask process is used to enable a Self-Aligned Via process that will be described. A low resistance Metal-9 redistribution layer is formed on top of the conventional on-die power distribution network. The Metal-9 layer uses Cu plate-up between sacrificial photoresist lines followed by spin coating of a polymer dielectric as described previously [2].

Process Discussion

The contact layer in the process has been optimized to minimize line resistance and support high current densities required for high-performance products. The on-die Metal-1 to Metal-7 interconnects are formed by dual damascene patterning with highly manufacturable low-k CDO dielectrics. At the lowest 3 layers, a CDO film has been chosen with the k reduced by a further 5% from previously published work [2] to improve the capacitance scaling. The lower layer metal pitches are 112.5nm, while upper layer metal pitches increase progressively to optimize density and performance as detailed in Table 1. These lower layers also have balanced resistance of the metal line and electromigration performance to reliably supply the high current densities required of high performance products without the added costs associated with extra layers dedicated to power delivery. Metal-8 is also formed by dual damascene patterning but PECVD SiO_2 is used as the dielectric film and the Metal-8 layer is covered with a thick PECVD silicon nitride film. A cross section of the Metal-1 to Metal-8 layers is shown in Figure 1. Metal-9 is formed using a plate up process. This Metal-9 layer has been optimized to increase the height and minimize resistance compared to previous generations, even as it is scaled to a tighter pitch to enable optimum routing. A SEM image of the Metal-9 line, Via-9 and base of the Cu bump can be seen in Figure 2. The bump pitch has also been scaled to provide optimum routing and I/O density.

Table 1: Layer material, pitch, thickness, and aspect ratio

Layer	Dielectric Material	Pitch (nm)	Thick (nm)	Aspect Ratio
Contact	Oxide	112.5	100	
Metal 1	Lower k	112.5	95	1.7
Metal 2	Lower k	112.5	95	1.7
Metal 3	Lower k	112.5	95	1.7
Metal 4	Low k	168.8	151	1.8
Metal 5	Low k	225.0	204	1.8
Metal 6	Low k	337.6	303	1.8
Metal 7	Low k	450.1	388	1.7
Metal 8	SiO_2	566.5	504	1.8
Metal 9	Polymer	19.4um	8µm	1.5

The tightest pitch layers in the stack are patterned using a new process to High-Volume Manufacturing (HVM) called Self-Aligned Vias (SAV). In standard dual damascene processing, the vias are first created in the ILD, followed by metal line patterning, and then filled with a metallic Cu barrier and then bulk Cu, and planarized. A significant challenge at these tight metal line pitches is to enable via patterning without having via-metal shorts that degrade die yield. This can be achieved by requiring exceedingly tight via layer-to-metal layer alignment in the lithography process, but this becomes expensive in HVM. Another alterative is to have very small vias, but this leads to degradation of photolithography capability and negatively impacts

electromigration (EM). In addition, since the vias are patterned first in the ILD, they are subjected to the metal etch and cleans in addition to the via etch and cleans, and this can increase the via dimensions and aggravates the via-to-metal shorting problem. Via-first processing also can allow the CDO to be damaged by the extra processing in contact with the ILD surface. A typical top-down SEM result of a via-first dual damascene process is shown in Figure 3. Note the very large via CDs and small via-to-metal shorting margin. This process is susceptible to metal-to-via misalignment.

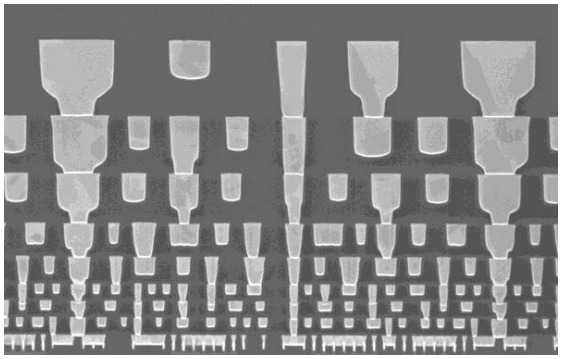

Figure 1: SEM image of 32nm interconnects to Metal-8.

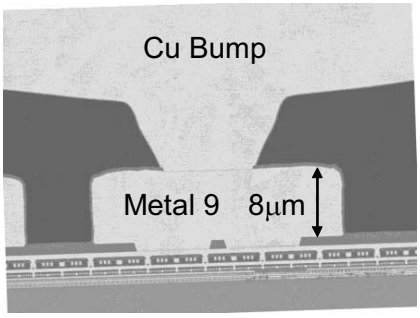

Figure 2: SEM image of 32nm interconnect for M9-bump.

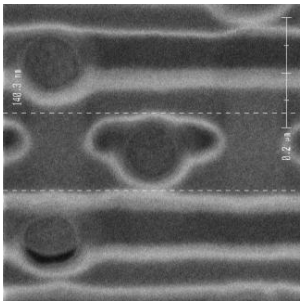

Figure 3: Top-down SEM image of a patterned via-first process showing tight via-to-metal shorting margin.

In the SAV process, the ILD is deposited followed by a blanket hardmask deposition. The photolithography defines the pattern for the metal lines, followed by dry etches to pattern these lines through the hardmask layer and then cleans to remove remaining resist and etch polymers. After metal line patterning is complete, the via photoresist pattern is overlayed onto the hardmask lines and etched into the ILD. The via etch is designed to only etch the ILD and not etch the hardmask, leaving it intact, and forming vias only where the metal lines were previously patterned. This results in vias that are well-aligned with the metal line patterning and having small encroachment into the space between metal lines. A final etch process completes the trench and via patterning to reach the SiCN etch stop layer and define the trench depth. A schematic of this process flow is shown in Figure 4. A top down SEM image showing the significant improvement for via dimension control by SAV is shown after patterning and after metal fill and chemical mechanical polish (CMP) in Figure 5. SAV shows excellent alignment of vias to the metal line patterning and good CD control.

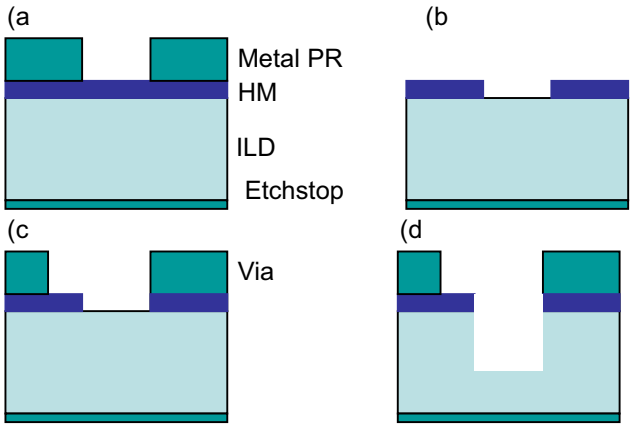

Figure 4: SAV process flow: (a) metal line resist is patterned, (b) metal pattern is etched into hardmask, (c) via resist is patterned, and (d) via is etched into ILD

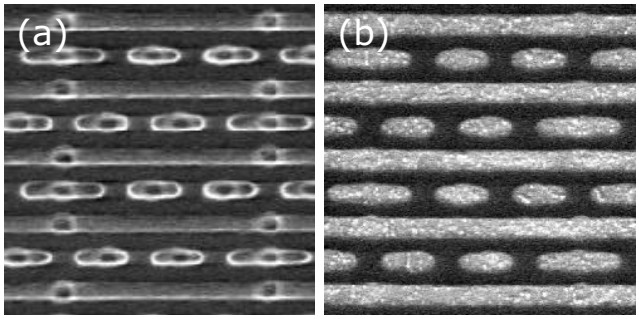

Figure 5: (a) Topdown SEM images of SAV process after patterning, and (b) after metal fill and CMP.

Multiple via sizes are supported in with SAV as can be seen in the cross-section SEM image in Figure 6. Small vias are supported on minimum width lines to maximize layout density. Larger vias are supported on wider lines to support higher current densities. Excellent CD control of SAV and via etch selectivity to the hardmask enables the process to support a tighter minimum pitch via placement. Vias placed at minimum metal pitch can be formed by a single via resist opening as shown in Figure 7.

Results

The 32nm process delivers reduced capacitance relative to the previous 45nm process generation [2] through a combination of techniques. The lower-k CDO dielectric at M1-M3 support 5% lower capacitance at these layers. The reduced aspect ratio at these layers supports the requirement for ever lower line-to-line capacitance as well. Resistance at the tightest pitch metal layers includes a 10% resistance

penalty to enable high electromigration current density for high performance logic products. The mid-layer metals transition to somewhat looser pitches to support longer length metal routing and are optimized for lower resistance and while still maintaining good electromigration performance. The upper layers continue this trend by moving to the loosest pitch and lowest line resistance. Interconnect capacitance and resistance is measured for minimum pitch lines with 50% dense, minimum-pitch metal patterns directly above and below the measured feature. Total capacitance is the sum of line-line capacitance and layer-layer capacitance. Metal-2 RC results are shown in Figure 8 with median values of 0.2fF/um and 8 ohm/um at 112.5nm pitch.

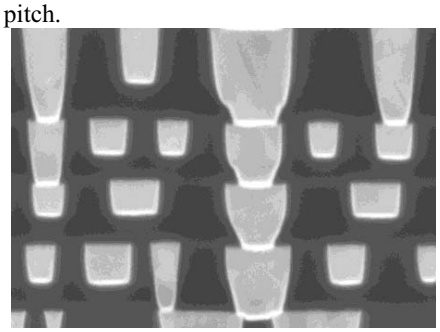

Figure 6: SEM cross-section of Metal-1 to Metal-4.

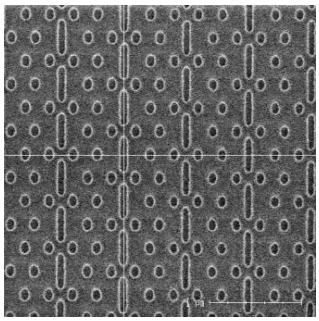

Figure 7: Top down SEM image of SAV via resist process.

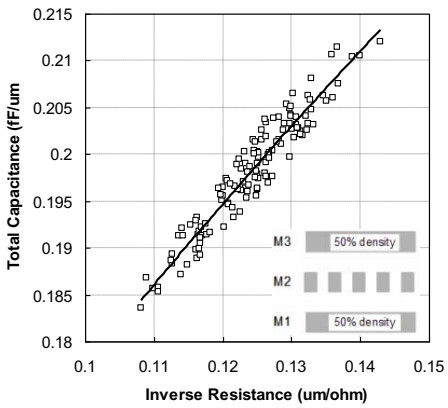

Figure 8: Metal-2 total capacitance vs. inverse resistance.

The electromigration reliability requirements for this technology have been carefully managed to deliver excellent reliability at the lowest possible metal line resistance. An important part of maintaining good RC at tight metal pitches is Cu-barrier film scaling to minimize the metal feature volume dedicated to the relatively high resistance barrier. This film has several additional requirements that must be simultaneously met: adhesion to the ILD and Cu, hermiticity, electromigration performance, and Cu diffusion control. A significant scaling of the barrier film was achieved for this technology node. In addition, the smaller top via CD obtained with SAV patterning process requires excellent Cu via fill. This has been produced with new Cu fill chemistries. Figure 9 shows a high resolution image of the M2 layer demonstrating the minimal barrier coverage and excellent metal fill without voids or other inclusions in the metal film. The electromigration performance of several Metal-2 wafers is shown in Figure 10. The process yields highly repeatable electromigration on multiple wafers.

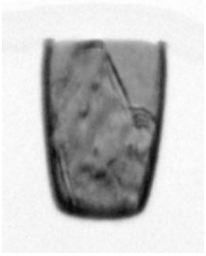

Figure 9: TEM of Metal-2 fill process showing the thin Cu barrier and excellent metal fill.

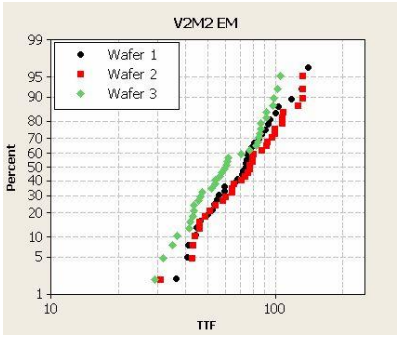

Figure 10: Metal-2 electromigration time-to-fail data for multiple wafers.

Summary

We have demonstrated a Cu interconnect with good RC and EM scaling for the 32nm technology node. This process has been developed with a new patterning process at the tightest pitch layers to enable good die yield. The metal fill process has been optimized for excellent electromigration performance and line resistance, as well as reduced capacitance from the 45nm technology.

Acknowledgements

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